



SUCCESS STORY



Siloti Visibility Enhancement Products Ease P.A. Semi's System Validation Burden

P.A. Semi Overview

P.A. Semi is a fabless semiconductor company based in Santa Clara, California. Founded in July 2003, it designs and develops microprocessor-based silicon system solutions for the high-performance embedded and computing markets. Its processor solutions achieve high performance at very low power consumption, and are optimized for embedded data communications, high-end consumer, portable, network, server blade, and telecommunications applications. Backed by an innovative architecture, patented technology, a world-class design team, and a broad ecosystem of development tools and software partners, P.A. Semi System-on-Chip (SoC) processors are redefining the cost, power and throughput efficiency in high-performance processing.

Next-Generation Processor Validation Poses Visibility Challenges

P.A. Semi's PWRficient family of 64-bit multicore processors boast a tenfold advantage in performance-per-watt over existing processors and deliver up to 2.5-GHz per core at unprecedented low power (<http://www.pasemi.com/processors/index.html>). The PA6T-1682M PWRficient processor is a dual-core chip running at 2 GHz, with typical power dissipation in the range of 5 to 13 watts. Its ASIC core contains 20-million gates (excluding memory), multiple components and is primarily comprised of internally-designed intellectual property (IP). Due to its high level of complexity and integration, signal visibility during late-stage verification and system validation posed especially daunting tasks for the P.A. Semi verification team.

Traditionally, the verification team's approach revolved around the use of hardware emulation. According to Tse-Yu Yeh, director of architecture and verification at P.A. Semi, "Hardware emulation plays a very important role in our overall verification process. We bring it in early in the design phase to build emulation models, even before the RTL becomes totally stable. Granted, the emulation runs fast, but when we run a very large program it often takes hours and hours to get to the point of failure. Then we have to turn our attention to debug. This process can be error prone and takes a significant amount of time and resources. What we really needed was a means of having good observability into our design without negatively impacting performance or our design and verification resources."

An Improved Strategy

To address the observability problem head on, P.A. Semi adopted an industry standard top-down design flow that utilized a mix of electronic design automation (EDA) tools. This mix included Novas Siloti™ Visibility Enhancement (VE) products as well as the EVE ZeBu hardware-assisted verification platform.

The Siloti family of products addresses the costly problem of decreasing visibility into the functional operation of complex ICs during late-stage verification and system validation. Patent-pending visibility enhancement technology accelerates the process of understanding and repairing sources of erroneous behavior. Combined with Novas data expansion and abstraction correlation engines, Siloti VE products optimize verification while minimizing the impact



of observation. The net result is improved verification productivity and predictability.

With Siloti visibility enhancement, the P.A. Semi verification team accomplished two specific goals. The team was able to debug on the emulation platform prior to first silicon and, once the silicon was ready, it was able to extract necessary signal data and debug it in the context of the RTL description to better understand the behavior of the design.

Debug on the emulation platform

Prior to adopting the Siloti approach, P.A. Semi's verification team would debug by feeding small test cases into the EVE FPGA-based emulator platform. The resulting emulation dump would then be compared to the design's simulation dump. When a difference was found, the team had to figure out why it existed and what the associated problem was in the design. Unfortunately, the emulation platform alone did not provide the visibility into design behavior that P.A. Semi required. Suppose, for example, that the team wanted to stop emulation at the point of a failure and dump out data in an attempt to resolve the problem. The team would have to pre-build that capability into the FPGA, consuming precious real estate.

Siloti visibility enhancement offered the solution the P.A. Semi verification team needed to address this dilemma. According to Mike Dickman, principal engineer in charge of testing platforms at P.A. Semi, "We used Siloti to test emulation and to debug failures directly in emulation, without a simulation dump. This allowed us to zoom in on problems quickly—within a day or so. By comparison, if we had run a lone application or operating system, it would have taken us anywhere from days to more than a week to run instructions in the simulation model and get enough significant information via a signal dump to perform debug."

The Siloti products take limited signal data from emulation and automatically regenerate missing data that can then be used in debug at either the gate or RTL level utilizing Novas' Verdi™ Automated Debug System. Specialized engines correlate and expand data on-demand during debug, so that the verification team can take advantage of the powerful visualization and automation capabilities in the Verdi system. Designers can easily extract, isolate and display relevant logic in flexible design views and automatically trace cause-and-effect relationships to better understand design behavior as well as the interactions between the design, assertions and testbench. (For more information on P.A. Semi's use of Verdi go to: http://www.novas.com/Customers/Success_Stories/PA_Semi/.)

In one case in particular, the P.A. Semi team came across a diode that failed in emulation, but passed in simulation. When the two dumps were compared, the gates didn't match up with the simulation. Using its traditional approach to debug, they would have been forced to manually examine the state elements and trace back through logic and time to find the source of the problem. Instead, using Siloti visibility enhancement techniques, limited signal data from the emulation dump was processed, missing signal data was regenerated, and all of the information was then correlated to RTL. Examining the RTL, the team quickly identified the source of the problem and was able to isolate and correct it in less than an hour.

Silicon Validation

Siloti improved PA Semi's non-destructive scan methodology—an approach that limits the area budget. Using Siloti essential signal analysis, the team was able to analyze observability tradeoffs to maximize overall signal visibility using specialized Design for Debug (DFD) logic with minimal impact on chip resources. During prototype operation, they were then able to probe a minimal set of signals and use Siloti to correlate these chip-level verification results back to RTL source and regenerate missing signal data on-the-fly so that the team could debug silicon operation in the familiar Verdi environment. This improved verification performance while providing full visibility into the design for a clear understanding of its behavior.

The decision to make Siloti visibility enhancement a key part of the company's system validation strategy was a straightforward decision for P.A. Semi. According to Mike Dickman, "We were a Siloti beta customer. It initially took us about a week to get up and running, but once we did the flow was very straightforward and fairly intuitive. It quickly became obvious to us that Siloti products offered access to a rich set of features that simply were not available with any other solutions on the market. The abstraction correlation feature allows us to map gates into RTL, while the on-the-fly data expansion capability enables us to quickly zero in on a particular branch where a failure occurs. With such a value proposition, we were able to meet our aggressive design goals as a start-up, while still maintaining our tight time-to-market schedule."

Siloti visibility enhancement continues to be a cornerstone of the system validation process established by the P.A. Semi verification team. Siloti products will have a leading role in the verification of single-core and quad-core versions of the PWRficient family of processors due out in early and late 2007, respectively. An eight-core version is planned for 2008.



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