



nTX Transaction Module

The Novas nTX™ Transaction module extends the Verdi™ Automated Debug System with advanced capabilities to extract, view, and analyze transactions. nTX's transaction capabilities simplify the process of understanding complex SoC operation by enabling debug and analysis at a higher level of abstraction.

nTX benefits include:

- Eases comprehension of complex protocols and buses
- Provides fast and flexible integration with a wide variety of verification environments
- Minimizes ramp up time for designs utilizing standard protocols
- Leverages standard SystemVerilog Assertion (SVA) syntax to describe and extract transactions for non-standard protocols

Debug at Higher Levels of Abstraction

Abstraction is an important technique in the verification, analysis, and debug of complex systems because it hides confusing, low-level details so engineers can focus on vital information about the operation of the system under test. Transactions abstract the communication between system or design components by using high-level operations rather than signal value changes. For “transaction-aware” environments, nTX provides flexible ways to capture existing transaction data for later debug and analysis. For environments that do not provide native support for transactions, nTX can infer them from signal-level activity. After the transaction data has been captured, nTX's debug and analysis features allow you to explore and understand design behavior and communication at a higher level of abstraction — eliminating the need to manually “reverse-engineer” system operation from complex, signal-level details.



nTX enables transaction-level analysis and debug of design operation and performance via waveforms, spreadsheets, and data-driven charts and graphs



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Transaction-level debug and analysis features include:

- Visualization and statistical analysis in waveforms, spreadsheets, graphs, and charts
- Specification and display of common and user-defined transaction relationships, such as parent/child or master/slave, in the waveform view
- Traversal of protocol stacks and hierarchies from top-level operation down to the signal-level details
- Support for complex transaction scenarios such as split or overlapping transactions
- Comparison of transaction streams captured from one or more designs in time-based or un-timed fashion
- Dumping and extraction capabilities to support a variety of transaction data sources

This comprehensive feature set provides complete support for common system-level applications and activities such as performance analysis, architecture optimization, and protocol debug, yet is fully accessible to RTL designers to enhance and speed the debug of the design implementation.

Support for Multiple Transaction Data Sources

Capturing transaction data into Novas' Fast Signal Database (FSDB) format is the first step to enable transaction-level viewing and analysis. Novas supplies technology to directly dump transaction data and the Novas nTX module provides two methods to extract transaction data:

Run-time Transaction Dumping to FSDB

- Native (direct) dumping from SystemC, SystemVerilog, and *e*
- Dumping from verification IP (Denali®, Spiritech®, and other vendors)
- User coding with an available C API

Post-process Transaction Extraction from FSDB

- Automatic extraction for the following standard protocols using a library based on Spiritech® transaction technology: AMBA_AHB; AMBA_AHB_lite; AMBA_APB; AMBA_AXI; MPEG2_TS; OCP_IP; PCIe; UART; USB 2.0
- User-definable extraction based on standard SystemVerilog Assertion (SVA) descriptions

Integration with Verdi

Because nTX is built on top of Verdi, it works seamlessly with all popular design and verification languages and tools. With the nTX module, Verdi provides a unified debug environment that leverages transactions to enable quick comprehension and analysis of complex SoC operation.