



# NOVAS

## Accelerating Engineers

SUCCESS STORY



## Verdi Debug System Key Element in P.A. Semi Verification Strategy

### Company Overview

P.A. Semi is a fabless semiconductor company based in Santa Clara, California. Founded in July 2003, it designs and develops the 64-bit PWRficient processor for the high-performance embedded, consumer and computing markets. Its processor solutions achieve high performance at very low power consumption, which makes them ideal solutions for embedded data communications, high-end consumer portable, network, server blade, and telecommunications applications. Backed by an innovative architecture, patented technology, a world-class design team, and a broad ecosystem of development tools and software partners, P.A. Semi System-on-Chip (SoC) processors are redefining the cost, power and throughput efficiency in high-performance processing.

### Next-Generation Processors Pose Powerful Development Challenges

P.A. Semi's PWRficient family of 64-bit multicore processors delivers high performance (up to 2.5 GHz per core) at unprecedented low power—a tenfold advantage in performance per watt over existing processors. Based on the Power Architecture from IBM, PWRficient processors uniquely integrate northbridge, southbridge and network-interface functionality into a single chip. Dubbed a platform processor, it is the first in its class to integrate what is typically a three to five-chip platform into a single chip. This high level of on-chip integration dramatically reduces the cost of silicon while delivering high throughput and low latency. As an added benefit, PWRficient processors flaunt a unique modular architecture that allows the cores, memory controllers, cache, SERDES lanes, and protocols to easily scale.

Developing the multicore, highly integrated SoC architecture compelled P.A. Semi's 150-engineer design team to confront a fundamental challenge in the industry today—delivering high performance processors with dramatically reduced power consumption. This was a driving factor for development of the first PWRficient platform processor, a dual-core chip running at 2 GHz with typical power dissipation in the range of 5 to 13 watts (depending on the application). The PA6T-1682M implementation features two DDR2 memory controllers and 2MB of L2 cache. A flexible I/O subsystem supports eight PCI Express controllers, two 10GbE XAUI controllers and four GbE SGMII controllers sharing 24 SERDES lanes.

In order to achieve the high level of performance it desired while dramatically reducing power consumption, the P.A. Semi team had to design a new, paradigm-shifting architecture from scratch. The team literally had to rethink every step in the design process as it attempted to achieve its breakthrough performance per-watt design.

Starting with the Power Architecture Specification from IBM, the team incorporated system requirements gathered from a large number of industry leaders in performance-embedded and performance-computing markets. The resulting 20-million gate ASIC and custom design (excluding memory), PA6T-1682M, is comprised of mostly internally designed intellectual property (IP) of the CPU, memory and IO interfaces. Due to its high complexity, multiple components and high level of integration, it posed a significant logic verification challenge for the team.



According to Tse-Yu Yeh, Director of Architecture and Verification at P.A. Semi, "The team's chief concern became how we would effectively deal with this complexity, debug as quickly as possible and ensure the design's quality while maintaining an aggressive start-up time-to-market schedule."

### **An Improved Debug Strategy**

To manage these challenges, Tse-Yu Yeh and his team adopted an industry standard top-down design flow that utilized a mix of electronic design automation (EDA) tools. This mix included the Novas Verdi™ Automated Debug System in addition to verification solutions from Cadence Design Systems, Denali Software, EVE-USA, Mentor Graphics, O-In Design Automation, and Synopsys, Inc. The team developed its testbenches in house using mostly C or C++. The Novas debug platform served as the key linchpin in unifying the debug/visualization capabilities of the disparate tools employed in the P.A. Semi design flow.

Including the Verdi tool as part of the company's verification strategy was a relatively easy decision for P.A. Semi. According to Tse-Yu Yeh, the Architecture and Verification team had previous experience using Novas' first-generation Debussy® Debug System to help improve debug productivity. "When we evaluated other possible debug systems, we found that Verdi had many capabilities and benefits that other solutions did not. And, because we were familiar with the feature navigation of Debussy, there was only a small learning curve for our engineering team. This ease of use enabled us to significantly cut design time."

In order to achieve the design goals set by the P.A. Semi engineering team, it needed an efficient way to gain a better understanding of design behavior. This was especially true given that the RTL code was written by a 20-person RTL development team, and thus must be debugged by a 20-person verification team.

The Verdi system provided the team with an intuitive way to analyze cause-and-effect relationships throughout their design. The tool automatically infers the logic functions of a design from its register-transfer-level (RTL) or gate-level description and interprets simulation results to generate an internal model of design behavior over time. With this information, the team could easily visualize design behavior, explore alternate scenarios and browse through unfamiliar code. As opposed to manually tracing back through the design statement-by-statement or gate-by-gate, the Verdi statement flow graphs automatically trace data and unknowns back through time. Its active annotation capability then allows variables to be viewed at the same point in both waveforms and source code.

Some of the Verdi features that Tse-Yu and his team found especially useful included advanced tracing capabilities and

the ability to effectively evaluate and justify whether or not they should trace code forward or backward over time to uncover the source of a potential problem. The schematic view of the RTL code also proved handy as the team worked on timing fixes of the design.

Another key Verdi feature that the team utilized is its ability to support the display and debug of PSL code for assertion debug. This allowed the team the flexibility to write PSL-based assertion properties, knowing full well that they would be supported by the Verdi system. They also used the open application programming interface supported by the Novas architecture to build custom tools for displaying the content of the pipeline. This tool worked with the Verdi register view to display the design's microarchitecture in the context of Verdi's other views.

Tse-Yu also sees the benefit of using Verdi on future projects. As he explains, "Tracing an unknown physical problem through a complex design during silicon debug is a process that can take an entire day. With Verdi, we will be able to narrow down a silicon problem in less than an hour. This will dramatically shorten the team's debug time and result in an order of magnitude productivity improvement. It will also help ensure that the P.A. Semi maintains its tight time-to-market schedule."

The P.A. Semi Architecture and Verification team continues to rely on the Verdi tool for much of its debug process. In addition to its role in the debug of its first processor, a dual-core device set to sample in Q3 of 2006, the unique capabilities and feature set of the Verdi tool will play a key role in the single-core and quad-core versions of the PWRficient family of processors due out in early and late 2007, respectively. An eight-core version is planned for 2008.

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